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Lateral MOSFET with contact structure

Abstract:

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(54) **Lateral MOSFET with contact structure.**

(57) A geometry for the metal contacts in a lateral MOSFET is disclosed. The cross-sectional shape of the metal contacts, which is usually six-sided but may also be a parallelogram, maximizes the cross-sectional area of the contacts while maintaining a required clearance from the gate layer and a required overhang of the lines in an overlying metal layer.

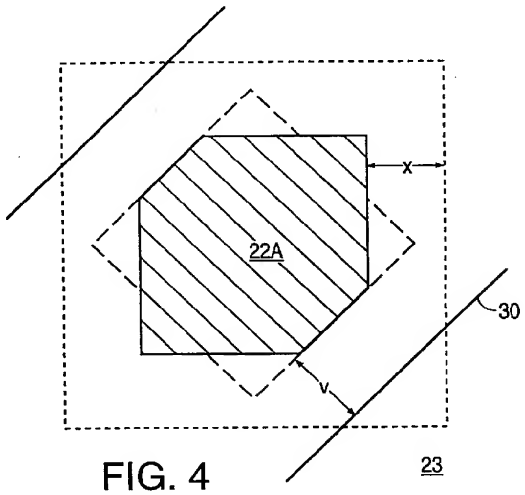

FIG. 4

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This invention relates to lateral MOSFETs, and in particular, to means for establishing contact between a metal layer and the source and drain cells of the MOSFET.

Reference is now made to Figures 1-3 of the accompanying drawings, in which:

Fig. 1 illustrates the layout of source and rain cells in a typical lateral MOSFET,

Figs. 2A and 2B illustrate top plan and cross-sectional views, respectively, of a cell in a typical lateral MOSFET, and

Fig. 3 illustrates a top plan view of a junction between a metal contact and a diagonal metal line.

In a lateral MOSFET, the source and drain diffusions are located on a single surface of a semiconductor substrate. While lateral MOSFETs can be constructed of long alternating stripes of source and drain regions separated by a gate stripe, it is well known that a closed cell arrangement typically provides a lower on-resistance in a given area. In such closed cell lateral MOSFET designs the cells are arranged in rows and columns as shown in Fig. 1, wherein cells alternate between source and design regions in both columns and rows. Source and drain metal interconnection lines are then deposited diagonally, such that the source and drain metal lines alternate with one another across the face of the chip.

Figs. 2A and 2B illustrate top and cross-sectional views, respectively, of a typical cell. In this example, a diffusion 20 of N+ type material is made in a P substrate 21. The N+ diffusion is accessed by a metal contact 22. The metal contact 22 is surrounded laterally by a layer of gate material 23, typically polysilicon, which is separated from the top surface of substrate 21 by a gate oxide layer 24. A thermal oxide layer 25 and a thick oxide layer 26 separate the polysilicon gate 23 from the metal contact 22.

To prevent a short between metal contact 22 and polysilicon gate 23, which would destroy the MOSFET, a minimal clearance, shown as "x" in Figs. 2A and 2B, must be maintained between them. If this minimal distance is not maintained, errors in alignment, for example, may create a short between the metal contact and the gate. A typical value of x is 1 μm. To minimize the on-resistance of the transistor, it is desirable to have the cross-sectional area of the metal contact 22 be as large as possible for a given size opening in the gate. Therefore, assuming that the opening in the polysilicon gate is a square, the cross-section of metal contact 22 would ordinarily be a smaller square separated from the gate by the minimal distance x on all sides.

Fig. 3 is a top plan view of a junction between the metal contact 22 and one of the diagonal metal lines, designated by the reference numeral 30, which illustrates the problem that occurs at this location. Metal contact 22 should be spaced a minimal distance from the edge of metal line 30, a distance which is designated as "v" in Fig. 3. Otherwise, a slight misalignment of the metal line may expose the contact. If the metal line does not cover the contact, then subsequent processing may etch holes through the silicon, destroying the junction and shorting out the device. It is well known that no portion of contact 22 should be left uncovered by metal line 30. As is evident from Fig. 3, metal 30 would have to be widened (see dashed lines 30A) to maintain the required separation between metal contact 22 and the edges of the meal line. This would very likely require that the source and drain cells be spaced further apart than is desirable fore minimizing the on-resistance of the MOSFET.

Alternatively, the minimal distance v could be maintained by rotating metal contact 22 through a 45° angle (as shown by the dashed lines). However, this will result in metal contact 22 being closer than the minimal distance x to the polysilicon gate 23. (The opening in gate 23 is illustrated by the dotted and dashed line in Fig. 3.)

In the metal contact structure of this invention, the cross-sectional area of the metal contact is maximized, while the minimal clearance between both the edge of the gate and the edge of a diagonal metal line is maintained.

According to this invention, a metal contact to a region of a lateral MOSFET is structured such that its corners which face the edges of an overlying diagonal metal line are truncated. This maximizes the cross-sectional area of the contact while maintaining minimal clearance between the edges of the gate and the metal line. The cross-sectional shape of metal contact is normally rectangular. By truncating the two opposite corners, a six-sided figure is formed, although the sides of the figure are not necessarily equal. In an extreme case, if the truncation goes all the way back to an adjacent corner of the rectangle, a parallelogram is formed.

This technique can be used in various types of MOSFETs, including those which have a body region separated from the source and drain cells, those which have a body region within each source cell, and those in which the drain cells are smaller than the source cells.

This technique can also be used in configuring vias which extend between diagonal metal lines and an overlying metal layer.

The invention is further described below, by way of example, with reference to Figures 4-15 of the accompanying drawings, in which:

Fig. 4 illustrates the six-sided cross-sectional shape of a metal contact in accordance with the invention.

Fig. 5 illustrates an alternative metal contact in accordance with the invention, whose cross-sectional shape is a parallelogram.

Figs. 6A and 6B illustrate a top plan view and a perspective view, respectively, of a conventional lat-

eral MOSFET without a local source/body short.

Figs. 7A and 7B illustrate a top plan view and a perspective view, respectively, of a conventional lateral MOSFET with a local source/body short.

Figs. 8A and 8B illustrate a top plan view and a perspective view, respectively, of a drain-enclosed lateral DMOS with a local source/body short.

Fig. 9 illustrates a perspective view of a drain-enclosed lateral DMOS wherein the gate layer does not extend the entire distance between the drain and the source/body cells.

Fig. 10 illustrates a drain-enclosed lateral DMOS in which the gate layer extends partially over a field oxide layer.

Fig. 11 illustrates a plan view of a lateral MOSFET in which the source/body cells are larger than the drain cells.

Fig. 12 illustrates a cross-sectional view of a lateral MOSFET cell including two overlying metal layers.

Fig. 13 illustrates a general plan view of the two metal layers.

Figs. 14A and 14B illustrate detailed plan views of a via between lines in the two metal layers.

Fig. 15 illustrates a pattern of vias used to interconnect diagonal metal lines to overlying vertical metal lines in accordance with another aspect of the invention.

Fig. 4 illustrates a top view of a metal contact in accordance with this invention. Metal contact 22A is similar to contact 22 (Fig. 3) except that the corners of the contact facing the edges of diagonal metal line 30 have been truncated. Thus the minimal distance x between the metal contact and the polysilicon gate 23 and the minimal distance v between the metal contact and the edge of metal line 30 have been maintained, while the cross-sectional area of metal contacts 22A has been maximized. Maximizing the cross-sectional area of metal contact 22A helps to minimize the on-resistance of the MOSFET. Truncating the corners of metal contact 22A eliminates the need to widen metal line 30. Although a wide metal line is desirable to minimize the metal line's contribution to the MOSFET's resistance and to maximize its current handling capability, a wide metal line is only desirable when it does not require larger spacings between devices. In a MOSFET, it is known that

$$R_{ds} \alpha \frac{L}{W}$$

where R_{ds} is the on-resistance of the MOSFET, L is the distance separating the sources and the drains (i.e., the channel length), and W is the total length of all drain edges which face sources. Avoiding the need to widen the metal line 30 allows one to maintain the cell separation L at a desired value, whereas if metal line 30 were widened the effect would be to increase L. Thus the overall effect of truncating the corners of metal contact 22A is to maintain R_{ds} at an minimum value.

The principles of this invention can be applied whether or not the diagonal metal lines are at a 45° angle with respect to the columns and rows of cells, and whether the opening in the gate layer is square or rectangular, or any other polygonal shape. Fig. 5 illustrates a gate layer 50 which has a rectangular opening and a metal line 51 which is oriented at an oblique angle other than 45° to the sides of the gate opening. As is apparent, in this situation truncating the corners of metal contact 52 may yield the shape of a parallelogram.

The broad principles of this application are applicable to a wide variety of lateral MOSFETs. Figs. 6-10 illustrate several of these possibilities.

Fig. 6A illustrates a top plan view and Fig. 6B illustrates a perspective view of a conventional lateral MOSFET with a remote body region. In this embodiment, the source and drain cells include N+ diffusions in a P substrate, and a P+ body contact diffusion is formed at the edge of the MOSFET. Whether or not the body is shorted to the source electrically depends on the circuit application. In any event, providing a P+ diffusion only at the periphery reduces cell size and thereby improves on-resistance (i.e., more cells/area).

Fig. 7A illustrates a top plan view and Fig. 7B a perspective view of a MOSFET which has a local P+ body region in each source cell. The source and body regions must be shorted, and this requires a larger metal contact than the source cells in the embodiment of Figs. 6A and 6B.

Fig. 8A illustrates a top plan view and Fig. 8B a perspective view of a drain-enclosed, lateral double diffused MOSFET (DMOS). In this embodiment, the substrate is N-type material, and the channel is formed in the P body region, which extends under the gate. Here the total distance between the cells is the summation of the width of the channel region (L) and the width (L_D) of a "drift" region which extends between the drain and the P body region. The metal contact must create a short between the source and body regions in each source/body cell.

Fig. 9 illustrates a perspective view of a lateral DMOS in which the gate does not cover the entire area between the source/body region and the drain region, i.e., the "drift" region is left largely uncovered by the gate. This reduces the electric field in the drift region, with the result that this embodiment allows a higher voltage than the embodiment shown in Figs. 8A and 8B.

Fig. 10 illustrates a perspective view of an embodiment similar to that shown in Fig. 9, except that the gate extends over a relatively thick field oxide. This further increases the capability of the MOSFET to withstand high voltages.

In the embodiment shown in Fig. 6, the metal contacts to the source and drain cells are essentially the

same size. In the embodiments shown in Figs. 7-10, however, the metal contacts extending to the source/body regions are normally somewhat larger than those which contact the drain regions. This type of arrangement is illustrated generally in the top view of Fig. 11, where a gate layer 80 has large openings 80S for the source/body cells and small openings 80D for the drain cells. Metal lines 81, 82 and 83 intersect the cells diagonally. The cross hatching indicates the metal contacts. As is apparent, the metal contacts in the source/body cells must be truncated to maintain a minimal distance from the edges of the metal lines whereas the metal contacts in the drain cells need not be truncated.

It is common to have a second metal layer above the diagonal metal lines. This overlying metal layer is separated from the metal lines by a dielectric except at locations where vias extend through the dielectric layer to allow contact between the two metal layers. A cross-sectional view of this structure is illustrated in Fig. 12 which shows a first metal layer 90 separated from a second layer 91 by a dielectric layer 92. A via 93 extends through dielectric layer 92 to make contact between metal layers between 90 and 91. Although in Fig. 12 via 93 is shown directly over the metal contact for purposes of illustration, in general it is common for the via to be spaced apart from the contact. Fig. 13 illustrates how contact might be made between diagonal lines of metal layer 90 and vertical lines of metal layer 91 to provide connections to drain and source terminals at the edges of the MOSFET. (The location of the vias are indicated by dots.)

Fig. 14A illustrates a detailed top view of a single intersection between a diagonal line of metal layer 90 and a vertical line of metal layer 91. A via 92 connects the two metal lines. As with the metal contact described above, it is important that via 92 not be left uncovered by errors of alignment or etching. Therefore, a margin "u" should be maintained between the edges of lines 90 and 91 and the perimeter of via 92. As Fig. 14A indicates, this yields a via whose cross-section is in the shape of a parallelogram. Alternatively, Fig. 14B illustrates a via 93 having a six-sided shape similar to the one shown previously for use with a contact. The advantage of a six-sided shape over the parallelogram of Fig. 14A is that it avoids acute angles, which may complicate the manufacture of photoresistors.

Illustrated in Fig. 15 is a plan view of a number of diagonal metal lines 100 in a first metal layer overlain by two vertical metal interconnect lines 101 and 102 in a second metal layer. Source and drain cells 103 (designated "S" and "D", respectively) and vias 104 (cross-hatched) extending between the first and second metal layers are also shown. It will be noted that along any given metal line 100, the cells 103 and vias 104 alternate, while the source cells are connected to interconnect line 101 and the drain cells are connected to interconnect line 102. This alternating via/contact layout minimizes the distance which current must flow exclusively in the first metal layer before reaching a via, thereby reducing metal resistance and current density in the metal lines 100.

Numerous alternatives of the embodiments described above will be apparent to those skilled in the art. All such alternative embodiments are intended to be within the scope of this invention, as defined in the following claims.

Claims

1. A lateral MOSFET comprising:

   a gate layer overlying a semiconductor substrate having a given conductivity,

   a plurality of cells arrayed in an orthogonal pattern on a surface of the substrate, each cell comprising a region of semiconductor material having a conductivity different in degree or polarity from the conductivity of the substrate, an opening in the gate layer, and a metal contact extending through the opening and making contact with the region of semiconductor material, and

   a first plurality of metal contact lines extending at an oblique angle to the orthogonal pattern, wherein at least some of the metal contacts have a cross-sectional shape which is designed to be as large as possible while maintaining at least a first predetermined minimal separation between the metal contact and the gate layer and at least a second predetermined separation between the metal contact and edges of one of the metal contact lines.

2. A lateral MOSFET as claimed in claim 1 wherein some of the cells are source cells, and wherein the MOSFET comprises a body region separated from the source cells.

3. A lateral MOSFET as claimed in claim 1 wherein some of the cells comprise a source region and a body region, the source region and the body region being shorted together.

4. A lateral MOSFET as claimed in claim 3 wherein some of the cells comprise a drain region, the opening in the gate layer in the cells which comprise a source region and body region is larger than the opening in the gate layer in the cells which comprise a drain region, and the cross-sectional shape of the metal contact in only the cells which comprise a source region and a body region is six-sided.

5. A lateral MOSFET as claimed in claim 1 wherein the substrate is of a first conductivity and wherein the cells include drain cells comprising a drain re-

gion of the first conductivity and source/body cells comprising a source region of first conductivity and a body region of a second conductivity, the substrate being doped to a lesser degree than the drain region.

6. A lateral MOSFET as claimed in claim 5 wherein the gate layer overlies substantially the entire area between the drain cells and the source/body cells.

7. A lateral MOSFET as claimed in claim 5 wherein the gate layer overlies a channel region included in the body region but overlies only a portion of the area between the drain cells and the source/body cells.

8. A lateral MOSFET as claimed in claim 5, 6 or 7 wherein part of the gate layer extends over a field oxide layer.

9. A lateral MOSFET as claimed in claim 5, 6, 7 or 8 wherein the source and body regions in the source/body cells are shorted, the opening in the gate layer in the cells which comprise a source region and a body region being larger than the opening in the gate layer in the cells which comprise a drain region, the cross-sectional shape of the metal contact in only the cells which comprise a source region and a body region being six-sided.

10. A lateral MOSFET as claimed in any one of claims 1-3 & 4-8 wherein, in at least some of the cells, the cross-sectional shape of the metal contact is six-sided.

11. A lateral MOSFET as claimed in any preceding claim wherein the shape of at least some of the openings in the gate layer is square.

12. A lateral MOSFET as claimed in any preceding claim comprising a second plurality of metal lines overlying, and oriented at an oblique angle to, the first plurality of metal lines, a dielectric layer separating the first and second plurality of metal lines, and vias extending through the dielectric layer to connect certain ones of the first plurality of lines to certain ones of the second plurality of lines.

13. A lateral MOSFET comprising:

a first metal line having metal contacts to a series of source or drain cells underlying the first metal line and separated from the first metal line by a dielectric layer;

a second metal line overlying the first metal line and separated from the first metal line by a dielectric layer; and

a series of vias extending between the first and second metal lines through the dielectric layer, the vias being positioned at locations between said cells.

14. A lateral MOSFET as claimed in claim 12 or 13 wherein the cross-sectional shape of the vias is a parallelogram or is six-sided.

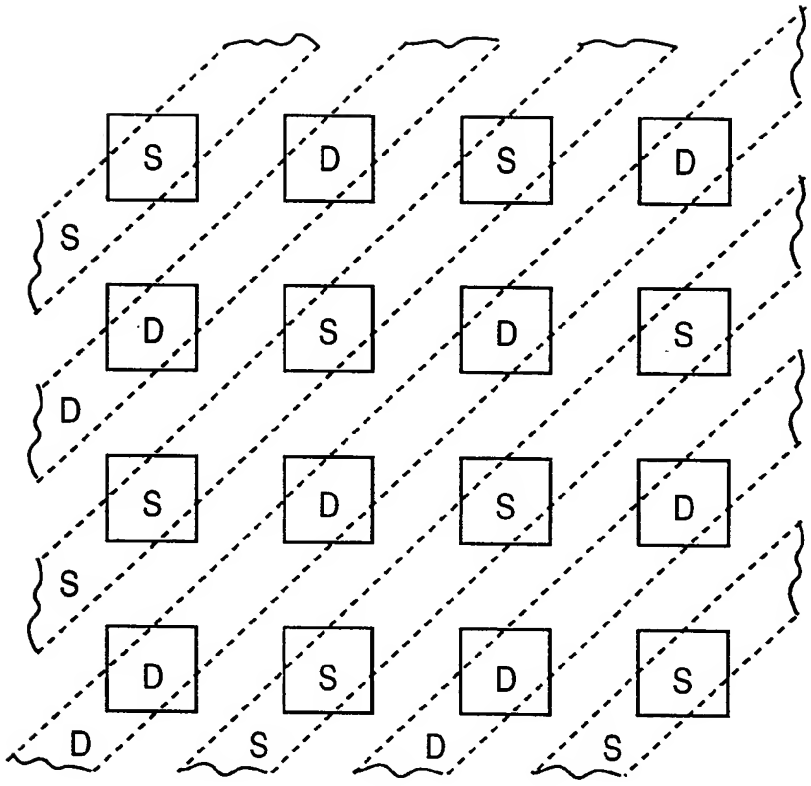

FIG. 1
(Prior Art)

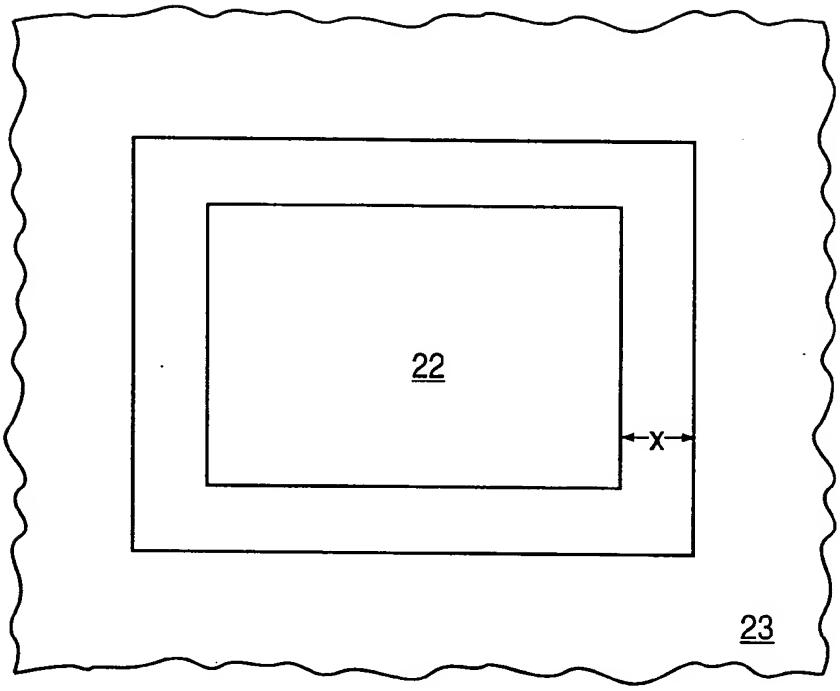

FIG. 2A

(Prior Art)

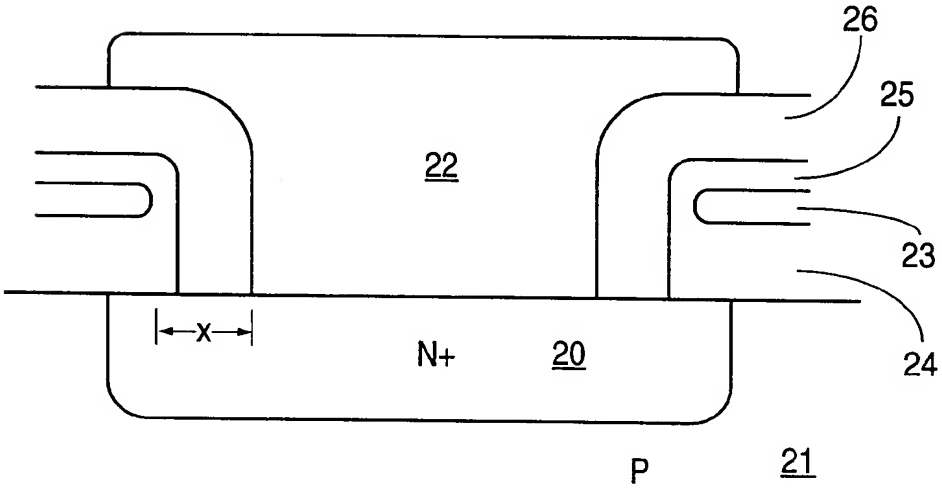

FIG. 2B

(Prior Art)

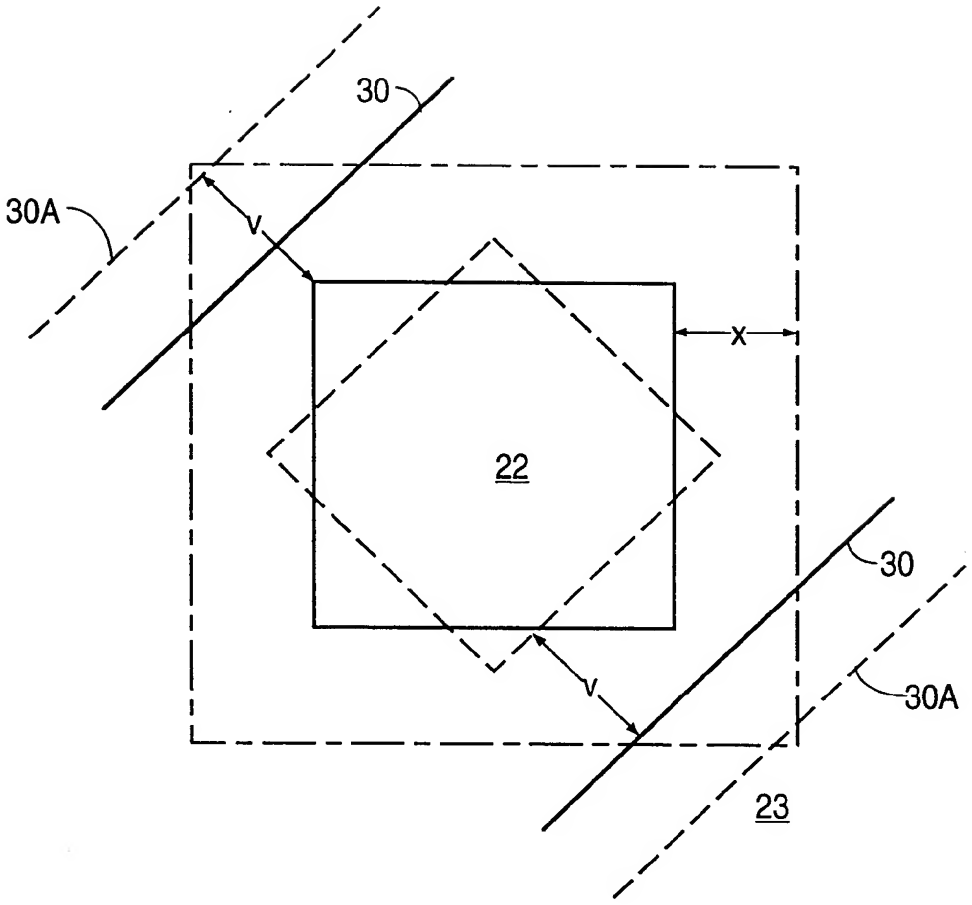

FIG. 3
(Prior Art)

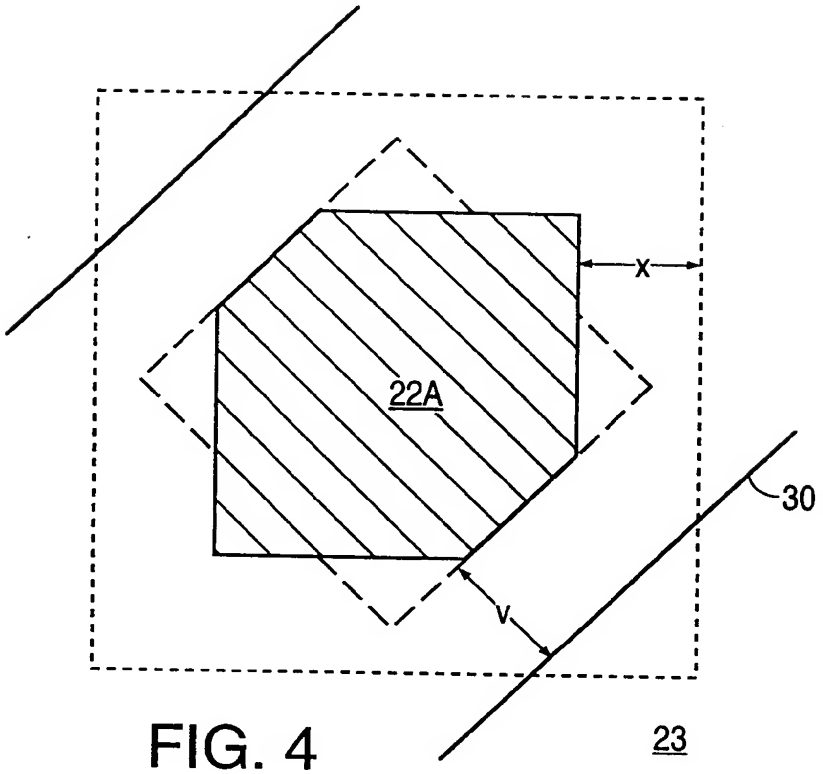

FIG. 4

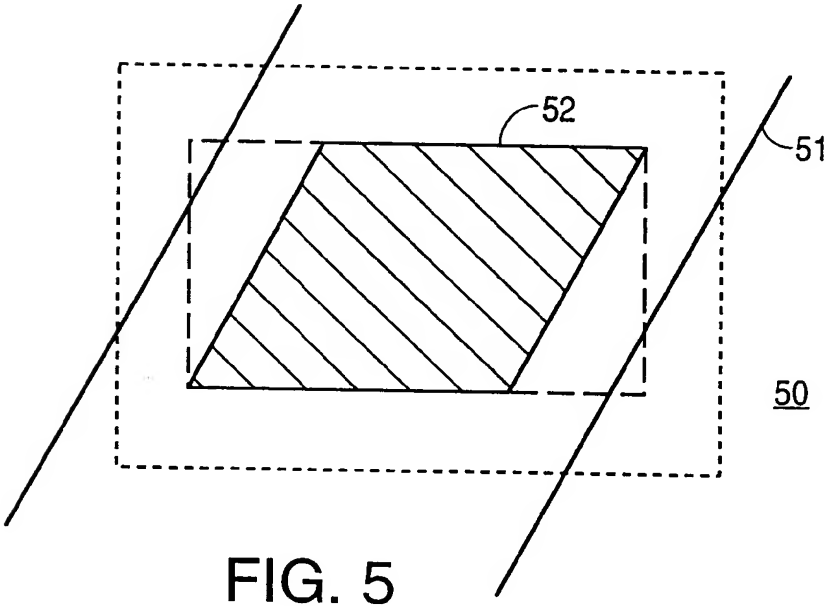

FIG. 5

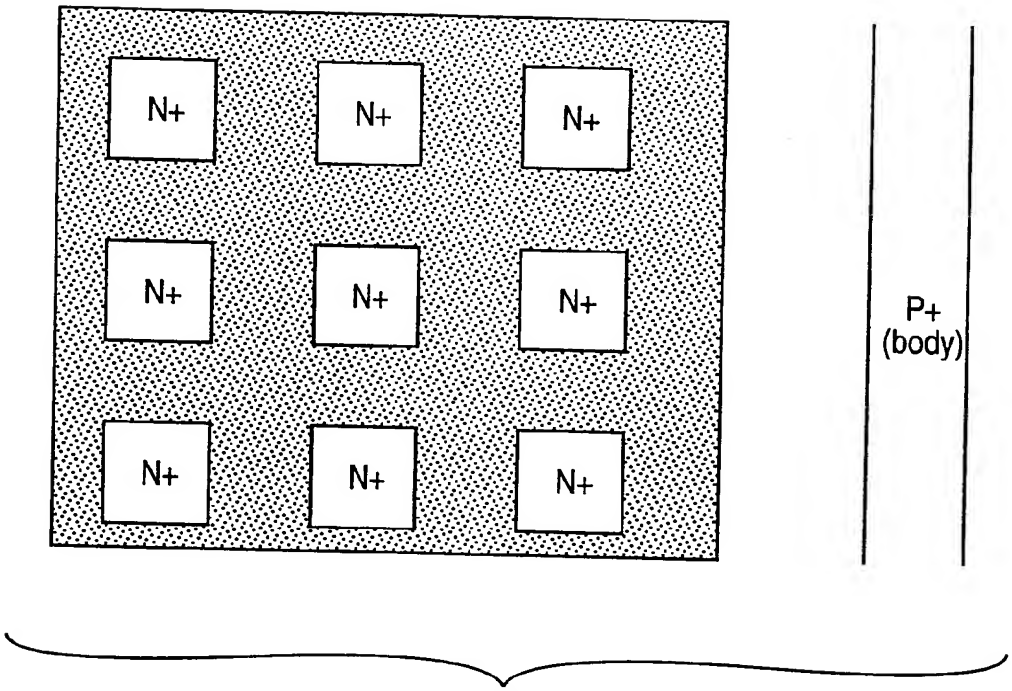

FIG. 6A

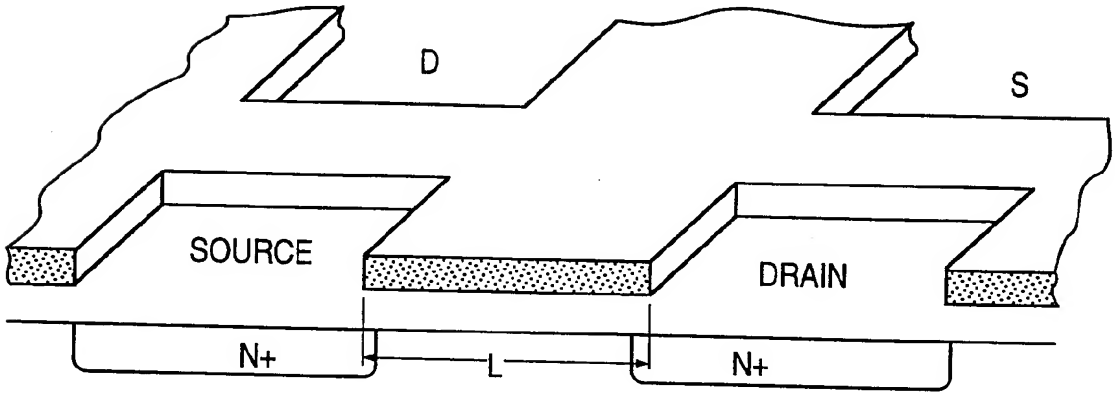

FIG. 6B

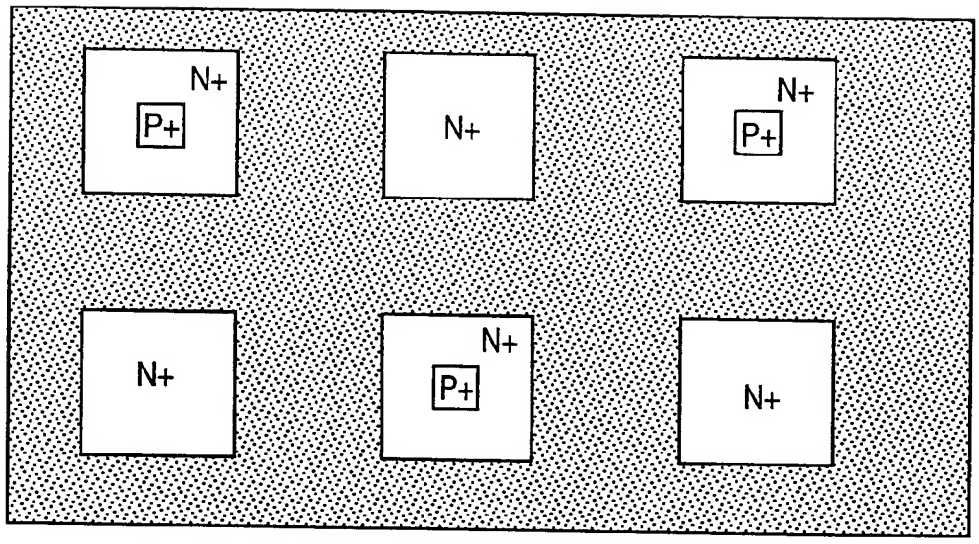

FIG. 7A

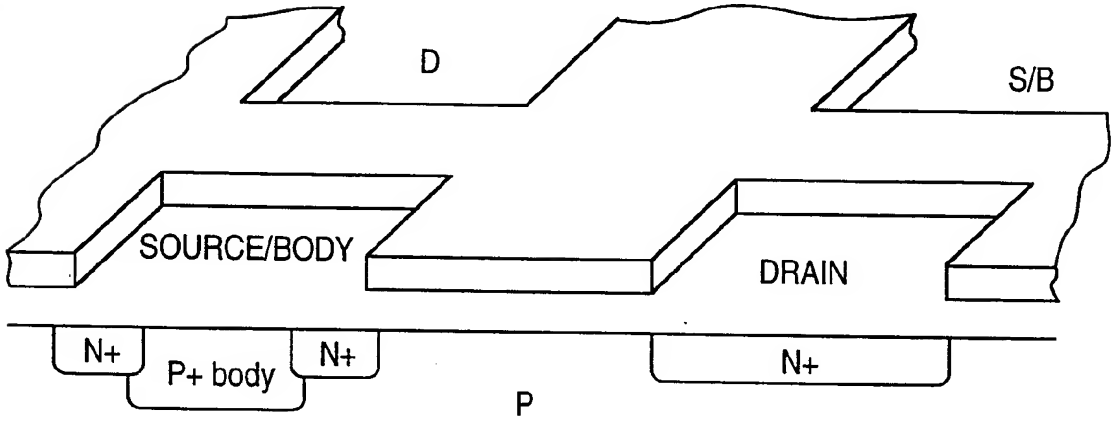

FIG. 7B

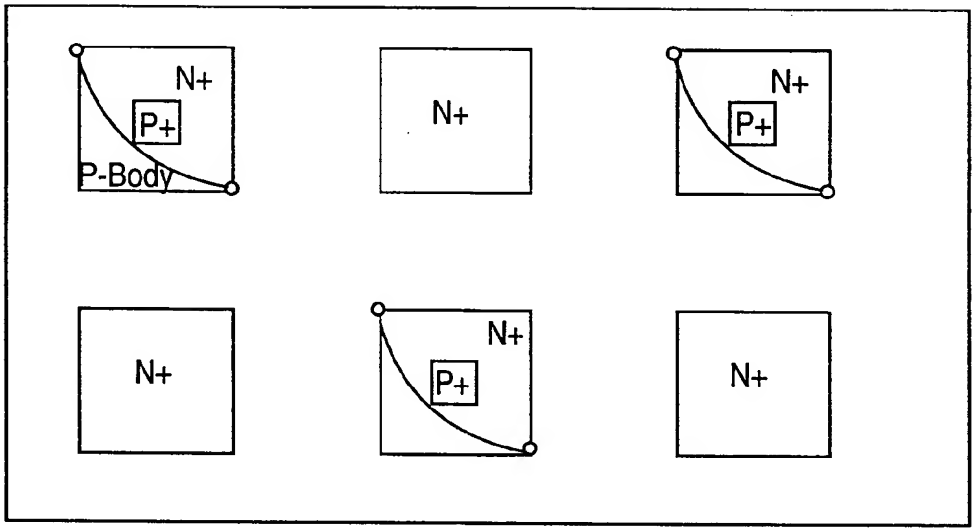
N+
P+
P-Body
N+
N+
P+
N+
N+
N+
P+
N+

FIG. 8A

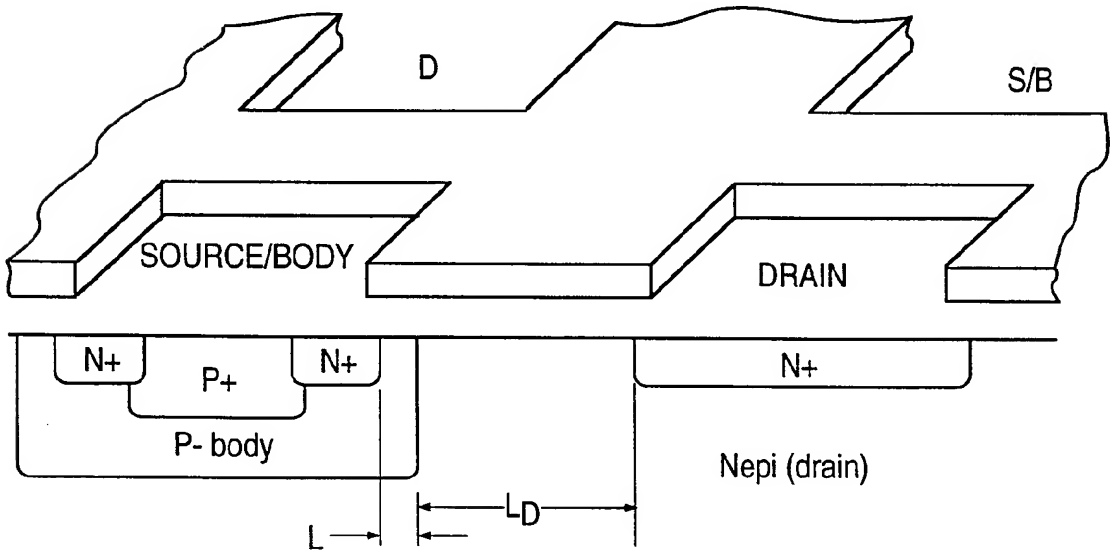
D
S/B
SOURCE/BODY
DRAIN
N+
P+
N+
N+
P- body
Nepi (drain)
L
LD

FIG. 8B

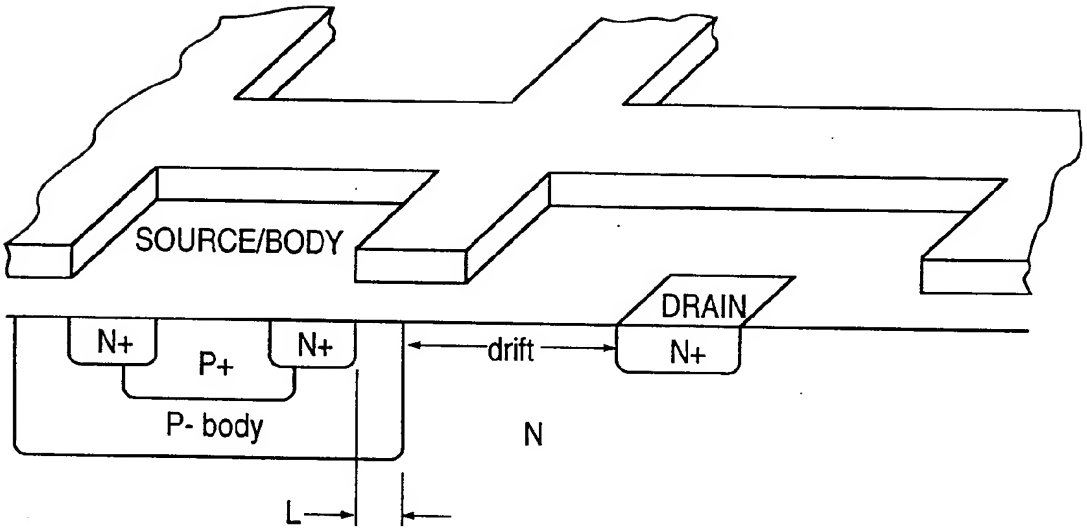
SOURCE/BODY
DRAIN
N+
P+
N+
drift
N+
P- body
N
L

FIG. 9

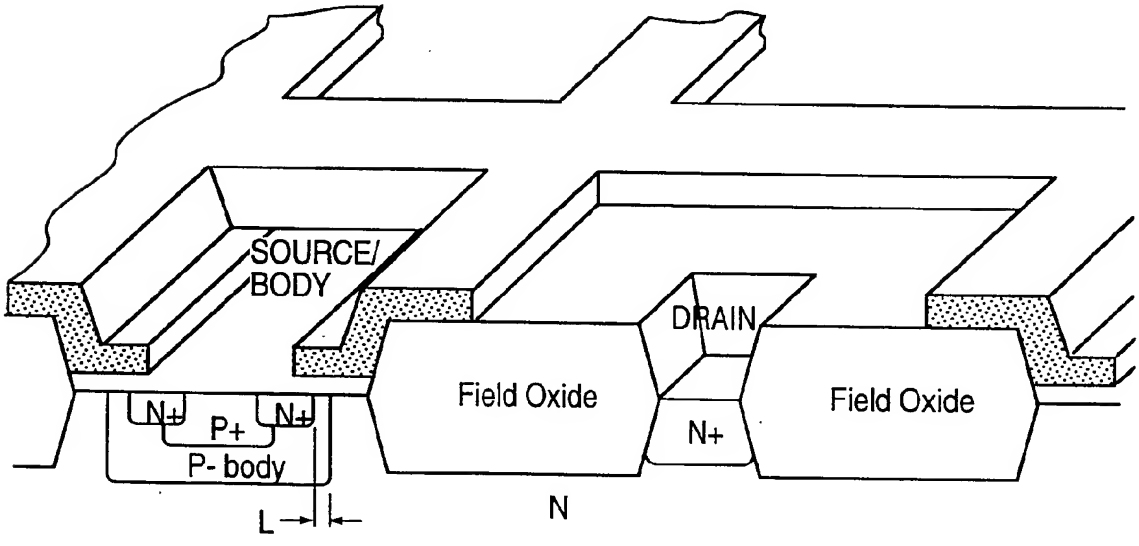
SOURCE/
BODY
DRAIN
Field Oxide
Field Oxide
N+
P+
N+
P- body
N
L

FIG. 10

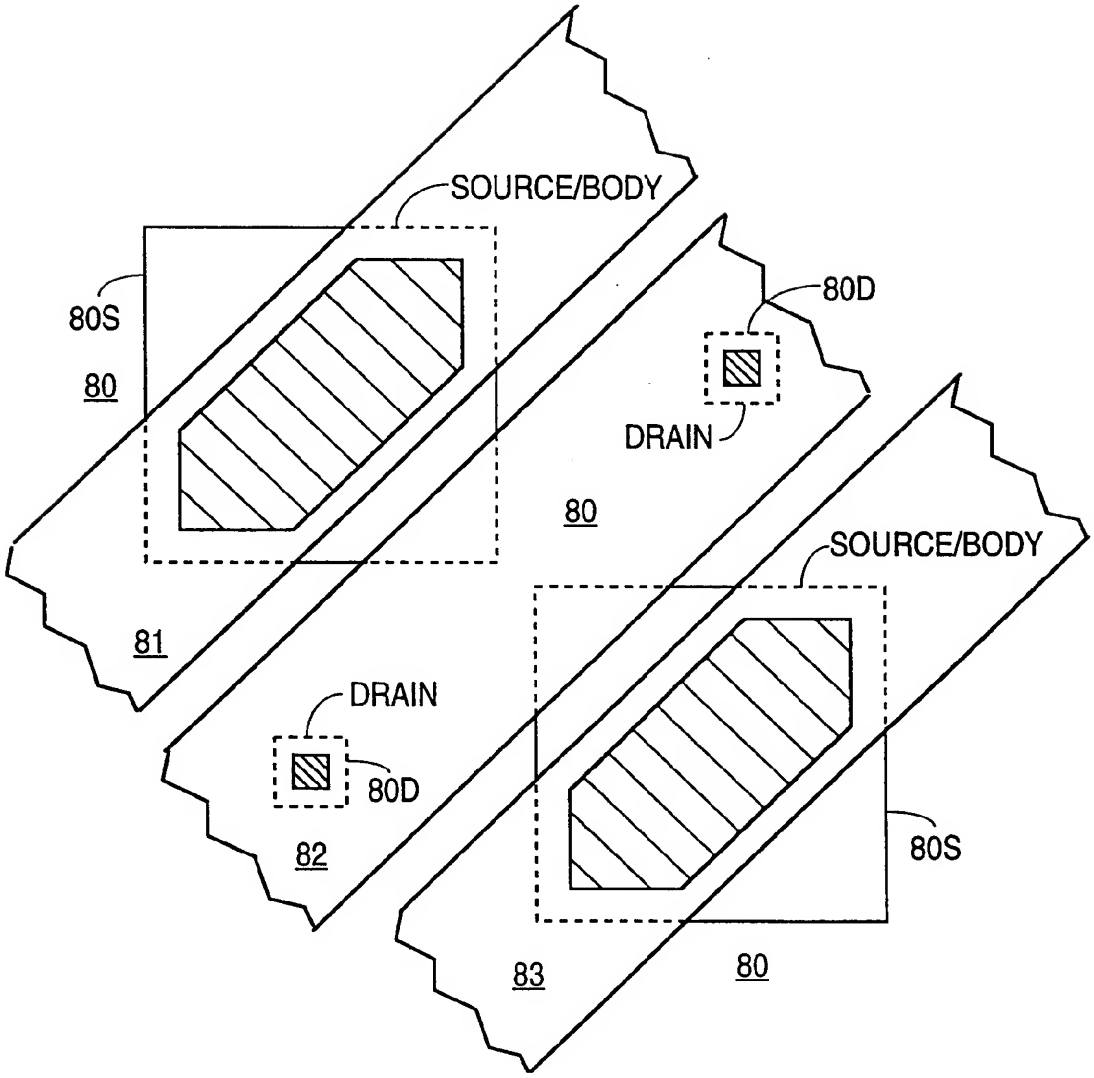
SOURCE/BODY
80S
80
80D
DRAIN
80
81
SOURCE/BODY
DRAIN
80D
82
80S
83
80

FIG. 11

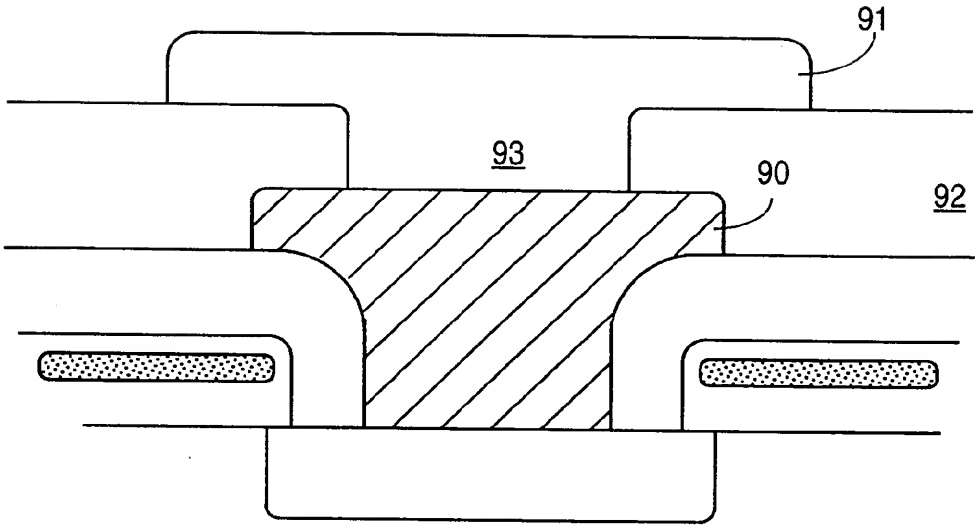

FIG. 12

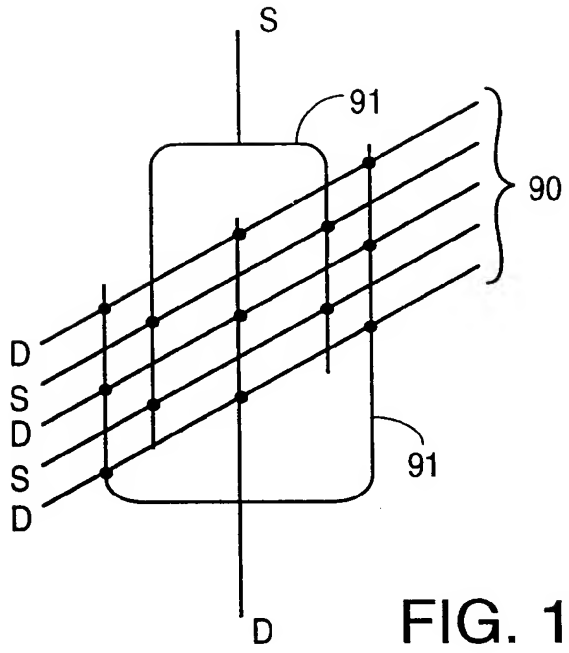

FIG. 13

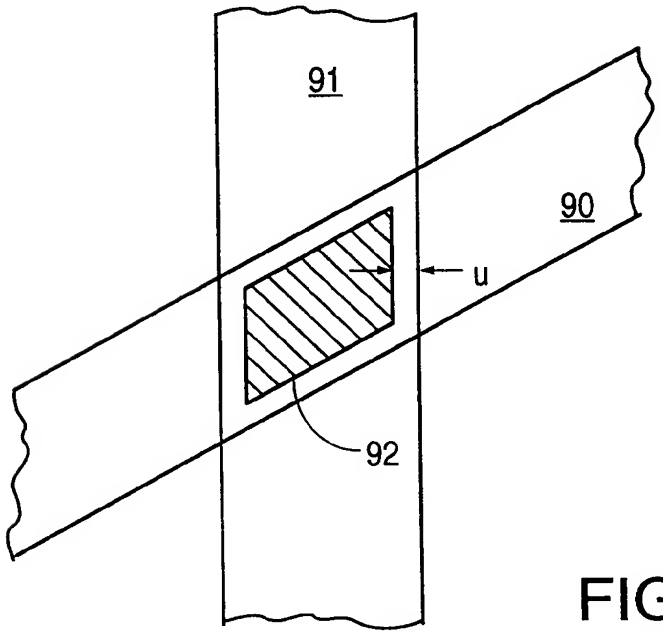

FIG. 14A

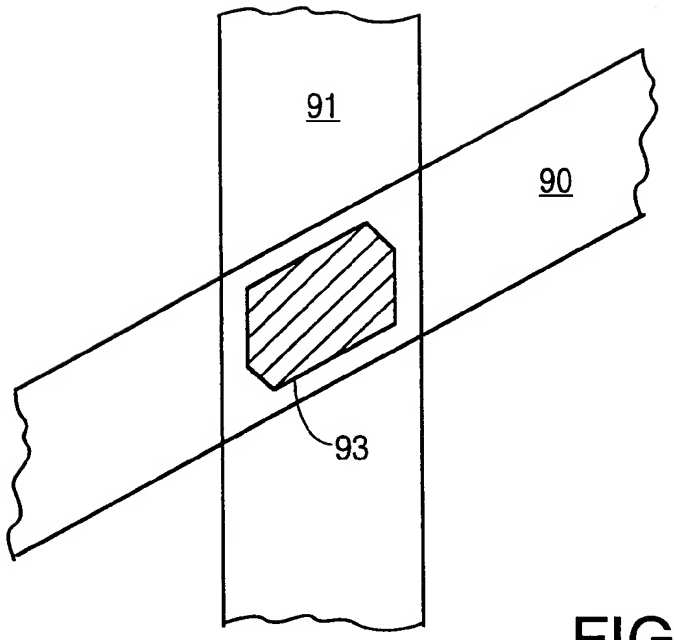

FIG. 14B

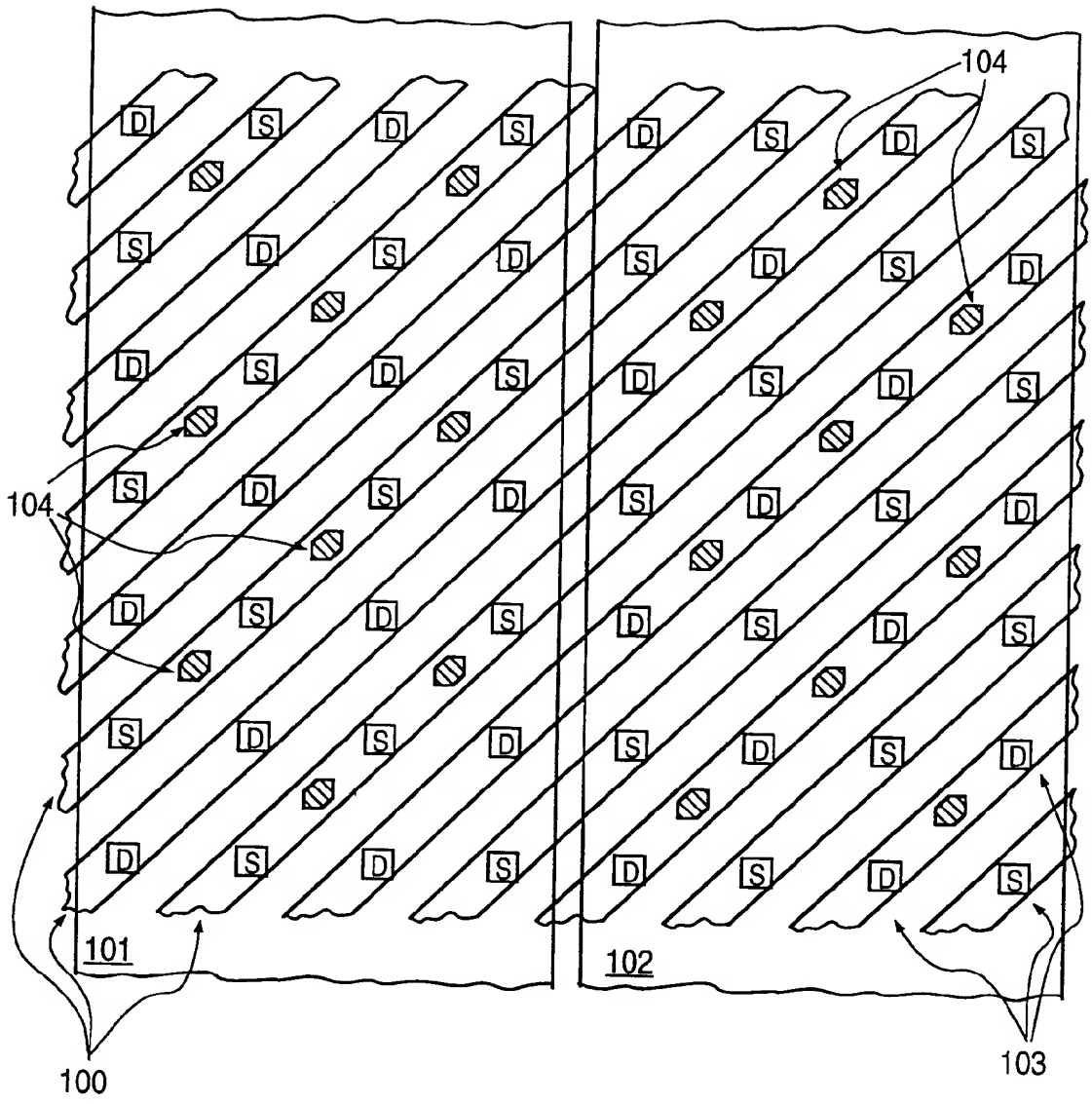

FIG. 15